

**V<sub>CE</sub> BREAKDOWN IS THE MAJOR CAUSE OF SEMICONDUCTOR-DEVICE FAILURE IN INDUCTIVE-LOAD CIRCUITS, BUT YOU CAN TAKE NUMEROUS STEPS TO PROTECT DEVICES FROM EXCESSIVE STRESS.**

# Techniques minimize switching-device failures in inductive circuits

**A**LL ELECTRONIC CIRCUITS GENERALLY use inductive elements, such as transformers, coils, or relays, and some applications, such as stepper motors, also have inductive loads. Unfortunately, the failure of switching devices in inductive circuits is a frequent problem and causes system failure. Switching-transistor and MOSFET failure is common in motor drivers, switched-mode power supplies, and similar electronic systems. The causes for the switch failures can be intrinsic or extrinsic. In an intrinsic failure, the device itself may be faulty, it may have undergone degradation, or it may have a latent defect that initial device testing did not detect. Extrinsic causes of failure include simply misapplying the device or making it operate beyond its safe-operating-area characteristic during normal operation of the system. In this case, the device is bound to fail due to excessive stress. The stress can be electrical (Figure 1) or thermal overstress.

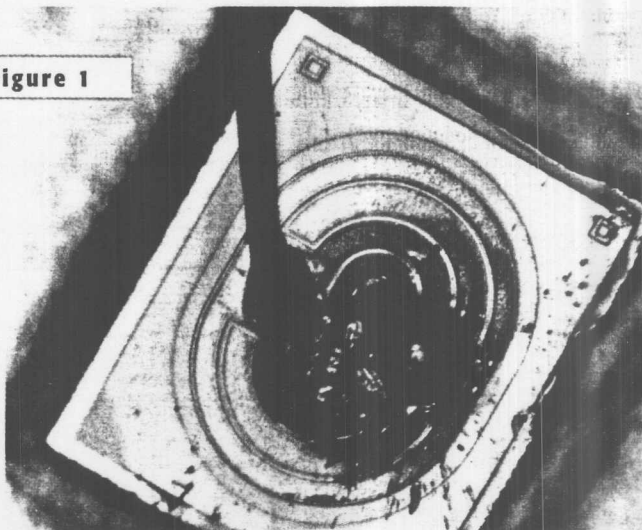
Minimizing switching-device failures in inductive circuits takes a multipronged approach. First, practice good design and construction techniques for transformers and other inductive elements in the circuit to reduce parasitics, such as leakage inductance and parasitic capacitance. Second, place protection networks or devices across the switching devices to protect against high-voltage breakdown. Third, use the appropriate switching device with a breakdown-voltage rating that's appropriate for the expected voltage levels in the circuit. You should derate by approximately 75% the breakdown-voltage rating that the data sheet specifies. You should specify acceptable leakage-inductance levels for all transformers and reject transformers that do not meet the specification during incoming inspection so that

such defective components do not later cause field failures. Because the reliability of any system depends on the reliability of every component in the system, paying attention to minor parameter details of transformers and switching devices greatly improves overall system reliability by reducing component failures.

## V<sub>CE</sub> BREAKDOWN CAUSES MOST FAILURES

V<sub>CE</sub> breakdown is the major cause of failure of semiconductor devices in circuits with inductive loads. Various reasons exist for the occurrence of this kind of failure. Whenever the voltage across the col-

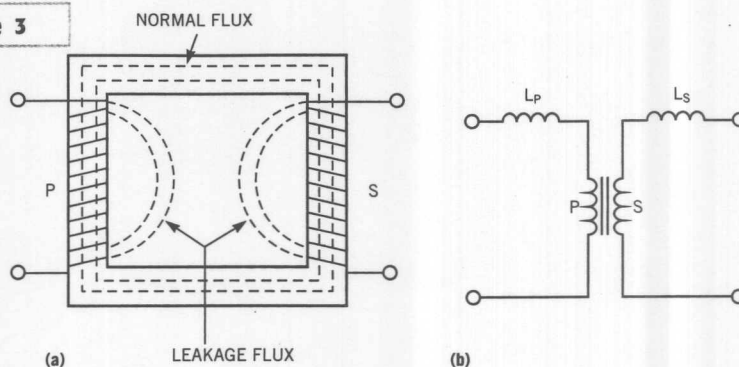
Figure 1



Electrical overstress severely damages a bipolar-junction transistor that operates in an inductive-load circuit—in this case, a switched-mode power supply.

vice,  $Q$ , to stress. The stress arises due to the  $L di/dt$  voltage that the abrupt changes in the current through the motor winding generate due to the fast switching action. This stress manifests itself in the form of a voltage, which the circuit impresses across the collector-emitter terminals of the transistor. If the amplitude of the voltage across the collector-emitter terminals of the transistor exceeds its  $V_{CE}$  rating, high-voltage breakdown of the collector-emitter junction of the transistor occurs. You cannot apply the full rating specified for  $V_{CE}$  or any other parameter to a transistor. You have to derate the specified ratings depending on the application's reliability requirements and the operating temperature. Generally, you should derate the  $V_{CE}$  rating by 75%. Therefore, if a transistor is rated to withstand a maximum of 100V between its collector and emitter terminals as per data-sheet specifications, its  $V_{CE}$  rating is only 75V. In any application, the  $V_{CE}$  of this transistor should not exceed 75V. The lower the ap-

**Figure 3**



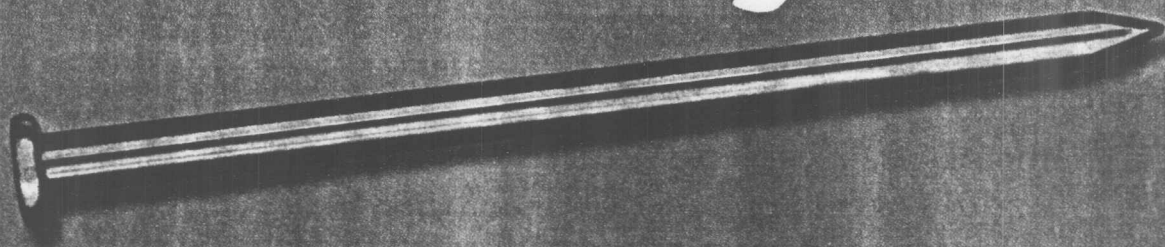
Leakage flux through air (a) causes leakage inductances  $L_p$  and  $L_s$  in the primary and secondary windings, respectively, of a transformer (b).

plied voltage between the collector-emitter terminals during normal operation of the system, the better the reliability of the system.

The first way to ensure the reliability of the system is to select a switching device that has a sufficient tolerance in

voltage ratings, especially  $V_{CE}$  breakdown voltage, depending on the application requirement. Then, apply the appropriate derating, such as 75% for  $V_{CE}$ . You can also protect a transistor in an inductive load circuit from  $V_{CE}$  breakdown by connecting a diode across the inductive load

# Jitter analysis?



**JitterPro +  
LC684**

**LeCroy**

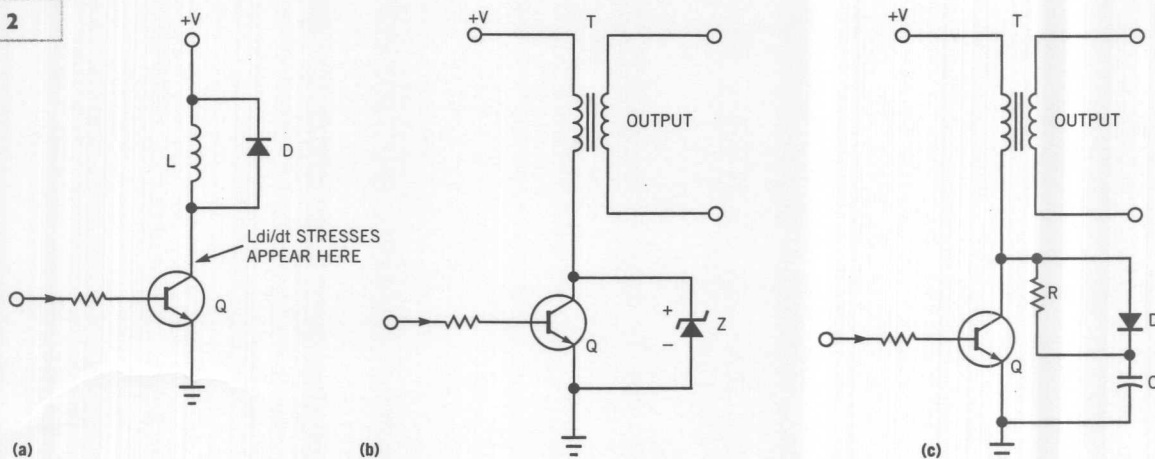
lector-emitter terminals of the transistor exceeds its rating, the device is likely to fail. Although designers select devices depending on the application requirement and the expected voltage excursions

in the circuit are likely to be within the  $V_{CE}$  rating, other elements in the circuit can cause the  $V_{CE}$  voltage to exceed the device's maximum limits.

Consider a basic transistor circuit in

which the transistor acts as a switch, turning a motor winding on and off (Figure 2a). In this circuit, the switching of the current in the inductive-motor winding subjects the switching de-

Figure 2



A diode protects the transistor from  $Ldi/dt$  switching spikes (a). A zener diode protects Q against  $V_{CE}$  breakdown (b). A snubber network protects Q from  $V_{CE}$  breakdown (c).

## SEALEVEL

SYSTEMS INCORPORATED

Combine multiport RS-232, RS-422, and RS-485 COM: boards with digital I/O boards to provide a complete solution for your communications and control tasks. PCI and ISA bus products are available to simplify installation. Drivers, utilities and sample programs are included for 32-bit Windows® and other operating systems.

# Another Simpler Solution.

Sealevel Systems combines software enhancements with comprehensive technical support to simplify your life.

© 1999 Sealevel Systems Incorporated

PCI LOCAL BUS



Sealevel Systems, Inc.  
PO Box 830, Liberty, SC 29657  
TEL: 864.843.4343 FAX: 864.843.3067  
EMAIL: support@sealevel.com

www.sealevel.com

Circle 4 or visit [www.ednmag.com/infoaccess.asp](http://www.ednmag.com/infoaccess.asp)



(Figure 2a), connecting a zener diode across the collector-emitter terminals of the transistor (Figure 2b), or connecting a snubber network across the switching device (Figure 2c).

In Figure 2a, Diode D provides a path for the current when the transistor turns off so that the decaying currents feed back to the power supply and the  $Ldi/dt$  spike does not cause stress across the collector-emitter terminals. This so-called freewheeling diode provides a free path for the decaying inductive currents when the switch is off.

In Figure 2b, the zener diode should have a breakdown voltage that's less than the transistor's  $V_{CE}$  breakdown rating so that the zener diode breaks down and conducts before a larger than normal voltage can damage the transistor. During normal operation, the zener diode does not conduct but rather breaks down when a larger than normal voltage appears at the transistor's collector. This zener diode, a so-called transient-suppressor diode, should have a fast re-

sponse. Also, the diode's power-handling capability should be high enough to withstand the stress when the diode clamps a high voltage and when the instantaneous power dissipation is high.

In Figure 2c, the snubber network consists of a resistor and a capacitor connected in series across the transistor with a diode connected across the resistor. This network prevents the circuit from exceeding the reverse-bias safe-operating-area characteristics of the device. The snubber network reduces the stress on the transistor during on/off cycles and reduces EMI problems by reducing the  $dv/dt$  at the collector. You should select the snubber components so that  $V_{CE}$  breakdown of the transistor does not occur when no signal is present at the base of the transistor.

You can use the following guidelines, which stem from simple and familiar equations, to calculate the snubber-component values. Referring to Figure 2c, the fundamental capacitor-charge equation gives the amount of charge that the snub-

ber capacitor stores, where  $Q$  is the charge,  $V$  is the voltage across the capacitor, and  $C$  is the capacitance of the capacitor:

$$q = Cv.$$

Differentiating with respect to time,  $t$ , gives the current, or the rate of change of charge:

$$\frac{dq}{dt} = C \frac{dv}{dt}.$$

Assuming 50% on and off times, the average current through the capacitor is  $I/2$ , where  $I$  is the full current. Thus,

$$C = \frac{I/2}{dv/dt} = \frac{I dt}{2 dv}.$$

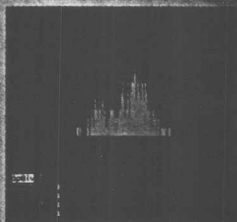
Over a full cycle,  $dt$  represents the fall time of the transistor's collector current. Remember that current flows through the capacitor only when the transistor is off. Thus, integrating the equation for  $C$  over a full cycle gives

$$2C \int dv = I \int dt.$$

# We've

## JitterPro™

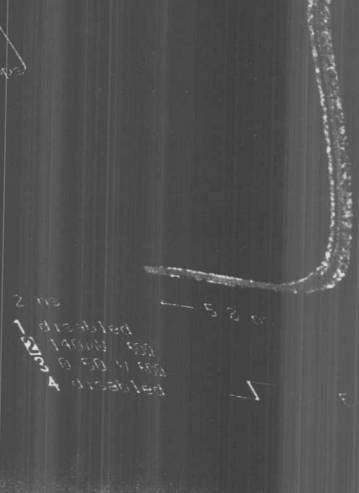
Here's the revolutionary new, comprehensive jitter and timing package that will knock others off the workbench. Only JitterPro gives you three views of jitter on a scope. JitterTrack™ (patent pending) shows the evolution of jitter over time. You can instantly spot the locations in the signal under test at which jitter violations occur and track them to their root cause. Or you can ask for a spectral view that shows the frequency components of jitter. Finally, you get an unmatched statistical view which can contain millions of measurements made from a continuous data set with zero deadtime. If you need to know the peak-to-peak jitter in a circuit, then you need 100,000 or more measurements to have statistical confidence. And JitterPro in combination with a high performance LeCroy scope is the most accurate and fastest way to get the answer.



Short memory scopes (100K) measure fewer edges. Smaller statistics can produce wrong answers!



Long memory scopes (up to 10M) process every edge, fast (no deadtime) to get the complete picture!



**LeCroy**

Therefore, the value of snubber capacitor C is as follows:

$$C = \frac{\frac{1}{2} \cdot t}{0.75 V_{CEO}} = \frac{I \cdot t}{1.5 V_{CEO}}$$

In this case, the voltage across the capacitor is approximately one diode drop lower than the voltage at the collector, and the equation includes a derating factor of 0.75 for the  $V_{CEO}$  rating of the transistor. When off, the transistor dissipates the energy that the capacitor stores. This energy is:

$$E = \frac{1}{2} CV^2$$

In other words, the power dissipated in the transistor when it is off is:

$$P = \frac{1}{2} C(0.75 V_{CEO})^2 f,$$

where f is the switching frequency of the transistor.

The RC time constant should be less than half of the on time of the transistor

so that the snubber network is ready to charge when the transistor is off. Using this rule, you can calculate snubber resistor R as

$$R = \frac{1}{2} \cdot \frac{t_{ON}}{C}$$

#### PARASITICS ALSO CAUSE PROBLEMS

In addition to  $V_{CE}$  breakdown, other problems, which commonly occur in switched-mode power supplies and other transformer-driven circuits, result from transformer parasitics. Leakage inductance and parasitic capacitance in the transformer are destructive parasitics that affect the reliable operation of the switching devices. A bad transformer can cause large power losses in a power supply due to parasitics. Normally, magnetic lines of force follow the magnetic circuit through the core between the primary and secondary windings. If the magnetic coupling between the primary and secondary windings is poor, magnetic lines of flux take other paths and

complete the magnetic circuit through the air between the windings (Figure 3a). This leakage flux gives rise to leakage inductance in the primary and secondary windings, which manifests itself as small series inductances in the primary and secondary windings (Figure 3b). Similarly, a parasitic capacitance exists between the primary and secondary windings of a transformer. Also, capacitance exists between the turns of the windings and between the layers in a winding. In combination with leakage inductances, the stray and other parasitic capacitances can form resonant circuits, which can cause voltage spikes in the output circuits. You can measure the leakage inductance by shorting the secondary winding and measuring the inductance of the primary winding at the operating frequency of the transformer. Leakage inductance depends on the construction of the transformer but is not highly dependent on the frequency.

These leakage inductances can cause large output spikes, which in turn can

# nailed it!

The JitterPro package, with its optional Clock Certification and Test Module (CCTM) for high speed clocks, is the first product designated by Rambus Inc. for certifying the jitter performance of DRCG (Direct Rambus® Clock Generator) clocks. But you don't have to be a scope expert to use it. Both JitterPro and CCTM contain a JitterWizard™ that steps you through the setup, acquisition and analysis of jitter. CCTM is specifically configured to make DRCG measurements easy by having default values that match the Rambus test procedures and an easy method to step through all the tests. Get fast, accurate measurements with confidence—you can really nail it with the 'Pro.

**RAMBUS  
SPECIFIED**

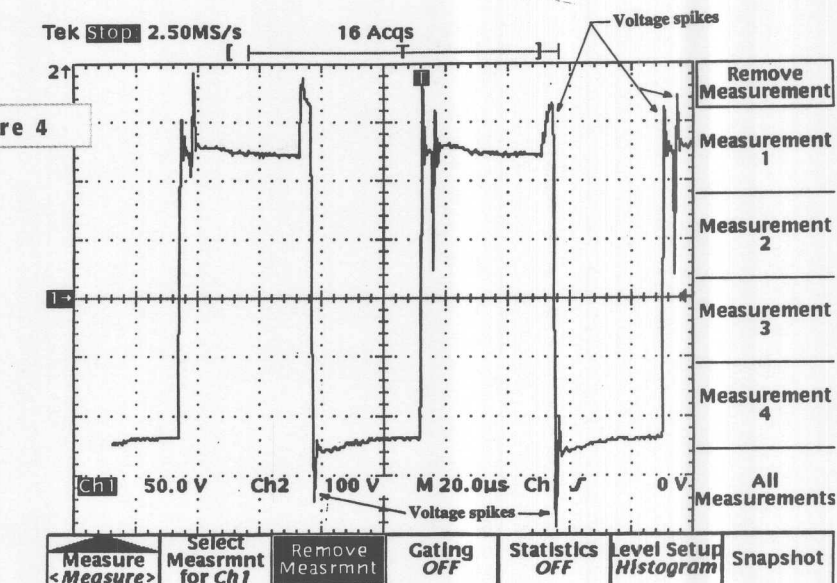
And built  
a better  
hammer too!

Introducing...



circuit failure. For example, in one recent case, a switching transistor in a transformer-based power-supply circuit was often failing. Large voltage spikes were observable at the output and the collector of the transistor, and the amplitude of the spikes was far above the normal switching waveform (Figure 4). Analysis of the mode of failure of the transistor revealed that the device had failed due to electrical overstress from collector-emitter breakdown (Figure 1). The amplitude of the voltage spikes exceeded the  $V_{CE}$  rating of the transistor, and, hence, the device had failed. Further analysis traced the cause of these voltage spikes to high leakage inductances in the transformer windings due to poor transformer construction and winding technique. Improving the transformer winding technique to reduce the leakage inductance corrected the problem.

Suitable transformer construction techniques include interspersing the primary and secondary windings to cover the



Voltage spikes are observable at the transition points of the collector waveform of the transistor.

whole bobbin and to ensure close proximity between the windings and placing an electrostatic screen between the primary and secondary windings.

Interspersing the windings and ensuring close proximity reduces flux leakage and results in better magnetic coupling between the windings. The key to reduc-

# LC684! See More!

Longm

## LeCroy's LC684 with JitterPro

The four new flagship DSOs from LeCroy are real powerhouses—with 8 GS/s maximum sampling rate, 1.5 GHz bandwidth and 16 megabytes of memory to accurately capture complex high-speed signals. You also get the best screen (10.4" TFT) to go with the best data-capture and -analysis capabilities in a high-speed scope. You can view up to four zooms of live waveform or math traces and zero right in on the problem. And you get the answers FAST. With the PowerPC® processor and up to 64 Mbytes of RAM in these new scopes, you'll get information up to 100 times faster than the competition.

8 GS/s SAMPLE RATE
16 MPT ACQUISITION MEMORY
2 PSEC ACCURACY*
1.5 GHz BANDWIDTH

\*Based on 100k samples

On the short-memory scope, the signal is aliasing and showing misleading information.

On the left, a scope with only 100k of acquisition memory attempts to capture a packet of data. The signal is badly undersampled. With such a short memory, fast ADCs are forced to run slowly when capturing complex signals. A LeCroy LC684DXL can acquire up to 16 million samples at 8 GS/s on a signal. Each sample (left screen) is now replaced by 160 samples (right screen) and the true signal shape is shown.

ing leakage inductance is maximizing magnetic coupling between the primary and secondary windings. In the interleaved winding technique, you place the secondary winding between two layers of primary winding. In other words, you wind the primary winding in two parts that lie on either side of the secondary winding. Another technique for achieving close magnetic coupling between the primary and secondary is to twist the wires together before winding the transformer; this winding technique is called bifilar winding.

An electrostatic screen generally consists of a copper foil wide enough to cover the full winding area; it connects to ground through a connection at the center of the windings. You can ensure that the two ends of the foil do not touch by placing an insulating material before the screen ends overlap. If the ends are not insulated, the shorted copper foil will act like a shorted single-turn secondary winding, and overheating may destroy this foil due to the excessive current in

## AN ELECTROSTATIC SCREEN GENERALLY CONSISTS OF A COPPER FOIL WIDE ENOUGH TO COVER THE FULL WINDING AREA.

this shorted foil, or "secondary." You ground the center point of the foil to cancel out the inductive effects due to the induced currents in the screen, which now flow in opposite directions to ground. □

### REFERENCES

1. Lowden, Eric, *Practical Transformer Design Handbook*, Howard W Sams & Co, 1985.
2. Billings, Keith H, *Switchmode Power Supply Handbook*, McGraw-Hill Inc, 1989.
3. Brown, Marty, *Power Supply Cook-*

book, Butterworth-Heinemann, 1994.

4. Brown, Marty, *Practical Switching Power Supply Design*, Academic Press, 1990.

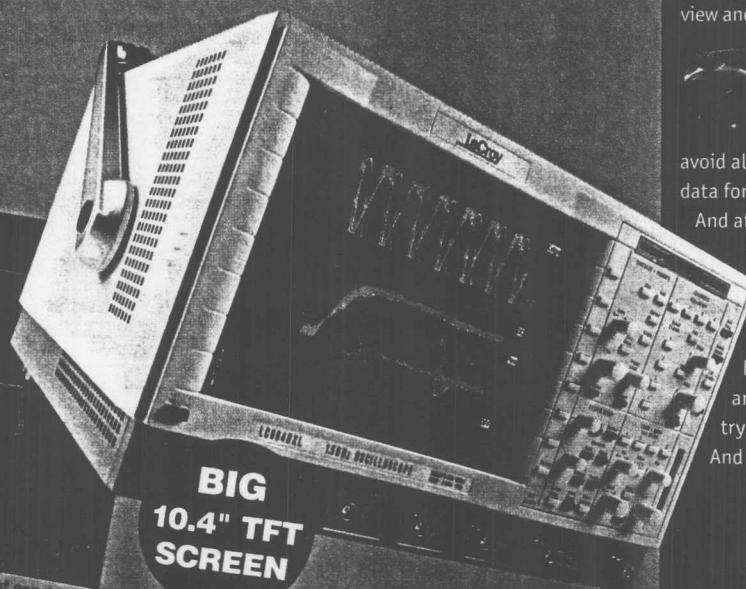
### ACKNOWLEDGEMENT

The author thanks YK Pandey, director of systems, and AK Manoj Kumar, senior program manager, Vendor Development Program, at the Centre for Development of Telematics (Bangalore, India), for their encouragement during this study.

### AUTHOR'S BIOGRAPHY

V Lakshminarayanan has an ME degree in Electrical Communication Engineering from the Indian Institute of Science (Bangalore, India). He has been working on the design and development of electronic systems for more than 16 years and is the coordinating engineer for failure analysis and reliability at the Centre for Development of Telematics (Bangalore, India). You can contact him at [vln@cdotb.ernet.in](mailto:vln@cdotb.ernet.in).

# ng memory drives it.



LeCroy's most powerful scope—with its big, flat, color screen AND the unique and affordable JitterPro software package - combine to help you capture, view and analyze complex signals more accurately. The long memory enables you to keep the sampling rate high, avoid aliasing and give you plenty of data for statistically accurate answers. And after you spot a problem, you get troubleshooting capabilities in the time, frequency and statistical domains. The intuitive menus really make this powerhouse combo easy to use. If you are a high speed circuit designer, try the LC684 and JitterPro combo. And hit the nail right on the head!

## LeCroy

1 800 4LeCroy [www.lecroy.com](http://www.lecroy.com)

The long-memory LC684 makes a single-shot acquisition of more information to produce a clearer picture. Don't be misled—see it all!

Circle 7 or visit [www.ednmag.com/infoaccess.asp](http://www.ednmag.com/infoaccess.asp)